# Intel® 82807AA Video Controller Hub

## Specification Update

***November 2002***

**Notice:** The Intel® 82807AA Video Controller Hub (VCH) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Order Number: 283656-002

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| 001 | Initial Release | June 2001 |
| 002 | Revisions include:<br>• Clarification to tables 19-22 titles only, contents of tables has not been changed<br>• Power sequencing timing clarification and calculation<br>• Clarification to the VCH GMBUS strapping<br>• Added Erratum #3<br>• Correction to table 18<br>• Clarification of LCD Enable bit VR01[2]<br>• Clarification of Panel Power Staus bit VR30[15] | November 2002 |

# Preface

This document is an update to the specifications contained in the *Intel® 82807AA Video Controller Hub (VCH) Datasheet*. It is intended for hardware system manufacturers and contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the 82807AA Video Controller Hub behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

## Component Identification via Programming Interface

The 82807AA Video Controller Hub may be identified by the following register contents:

| Stepping | Revision Number |
|---|---|
| A0 | VR00[11:8]=0000b |
| A1 | VR00[11:8]=0001b |
| A2 | VR00[11:8]=0010b |

# Component Marking Information

The 82807AA Video Controller Hub may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Notes |
|---|---|---|---|
| A1 | SL4QZ | FW82807AA | First production stepping |
| A2 | SL55P | FW82807AA | |

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed 82807AA Video Controller Hub steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| NoFix | There are no plans to fix this erratum. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |
| Shaded: | This item is either new or modified from the previous version of the document. |

| NO. | PLANS | ERRATA |
|---|---|---|
| 1 | No Fix | A Particular Combination of GPIO Values Causes VCH to Enter into Debug Mode for DVOr Interface |
| 2 | No Fix | VCH A2- LVDS serializer loses data stream synchronization |
| 3 | No Fix | VCH may violate panel power sequencing requirements |

| NO. | PLANS | SPECIFICATION CHANGES |
|---|---|---|
| 1 | Doc | Intel 82807AA VCH Revision VR00 register description |
| 2 | Doc | Change to CMOS panel interface drive strength |
| 3 | Doc | Change to Control registers VR31 and VR32 |
| 4 | Doc | Change to Control Register VR34 |
| 5 | Doc | Change to Timing Control |
| 6 | Doc | Change to Intel 82807AA VCH Panel Sequencing Diagram |
| 7 | Doc | Clarification to Control Registers VR31 and VR32, Power Sequencing |

| NO | PLANS | SPECIFICATION CLARIFICATION |
|---|---|---|
| 1 | Doc | Clarification to LVDS LCD Interface Pixel Data Serial Mapping Tables 19-22 Titles Only<br>Contents of tables has not been changed |
| 2 | Doc | Clarification to the VCH GMBUS strapping |
| 3 | Doc | Clarification of LCD Enable bit VR01[2] |
| 4 | Doc | Clarification of Panel Power Staus bit VR30[15] |

| NO. | PLANS | DOCUMENTATION CHANGES |
|---|---|---|
| 1 | Doc | Correction to Flat Panel Timing Diagram in doc SC-3088 rev1.0 figure 10 |
| 2 | Doc | Correction to Table 18. 18 bit CMOS uses same MSB's as 24 bit CMOS |

# Errata

### 1. A Particular Combination of GPIO Values Causes VCH to enter Into Debug Mode for DVOr Interface

**Issue:** If at any time the following combination of values is programmed into the VCH GPIO registers, VCH will enter a debug mode, and internal test-mode signals will be output onto the DVOr (DVO Replication Port) interface:

VR82[0] = 1 (GPIO2)
VR83[0] = 0 (GPIO3)
VR84[0] = 0 (GPIO4)
VR85[0] = 0 (GPIO5)
VR86[0] = 1 (GPIO6)

**Implication:** If the GPIO registers are set to the above values, the DVOr interface will undergo unexpected behavior.

**Workaround:** If normal operation of the DVOr interface is required, avoid programming the GPIO registers with the aforementioned combination of values.

**Status:** No fix

### 2. VCH A2- LVDS Serializer Loses Data Stream Synchronization

**Issue:** The VCH can enable and disable its panel interface under program control. If a VCH A2 device is instructed to disable (VR01[2]=0) and then enable (VR01[2]=1) without being powered down, the LVDS data stream can lose synchronization with the LVDS output transmit clock. This will result in the LVDS 7x data stream becoming shifted in phase with respect to the LVDS output transmit clock. Running certain test software ( such as WHQL HCT suspend.exe test) for an extended period of time(>8 hours) is more likely to inducing the serializer synchronization loss than running the system under normal operating condition. This issue should not occur on CMOS panels.

**Implication:** LVDS TFT displays in systems using the VCH A2 which experience this issue may show a variety of distorted display images (banding; horizontal/vertical roll; blank screen) when the VCH serializer loses synchronization. The LVDS data stream will stay out of synchronization from its reference LVDS output transmit clock until the host software issues a VCH LVDS block reset (by toggling VCH register VR12[1]). Systems using VCH A1 or earlier stepping are not shown this symptom. Likewise, VCH A2-based systems which use CMOS displays do not demonstrate the display image distortion seen on LVDS panels.

**Workaround:** Systems using VCH A2 with LVDS panels should include code which toggles VCH register VR12[1] to reset the LVDS block prior to enabling VCH operation. A reference video BIOS (2344 or later) which performs this bit toggling is available to OEMs. OEMs may contact their Intel field representative for access to video BIOS revision 2344 or later.

**Status:** No hardware fix.

### 3. VCH may violate panel power sequencing requirements

**Issue:** The VCH may violate panel power sequencing specs if the VCH receives a panel power-off command while it is still in a panel power-on sequence where the EnaBkl signal has not yet been asserted.

**Implication:** 830 and 815EM systems using the VCH may violate panel power sequencing or panel protection specs after suspend/resume, hibernate/wake, or display hot-key switching. If a panel power-off command is received before the EnaBkl signal has been asserted, the power sequencing timers in the VCH may be disrupted causing a subsequent panel power-off sequencing violation and/or a panel protection violation for the next panel power-on sequence. VCH Register bits VR01[02] and VR30[15] are not sufficient indicators to determine the current power sequencing state of the VCH.

- No visible indicator of panel violation
- LCD_VDD, BKL_EN, LVDS_CLK must be measured to detect violation

**Workaround:** Software should do the following:

- When setting VR01[2] to 1, software must assume a 25 millisecond delay from the time the command is executed in code to the rise of $ENAV_{DD}$.
- Code should not reset VR01[2] until completion of the panel power on sequence. ENABKL must be active before changing VR01[2] from 1 to 0.
- Software should account for any Tstay value to determine the completion of the panel power off sequence after VR30[15] is cleared (set to “0”).

A reference video BIOS (2661 or later) and Driver (11.03 or later) which incorporate these changes is available to OEMs. OEMs may contact their Intel field representative for access to video BIOS and Drivers.

**Status:** No hardware fix

# Specification Changes

## 1. Intel 82807AA VCH Revision VR00 Register Description

*Section 6.1.1.1. (Page 35) should be replaced by:*

### VR00 – 82807AA VCH Revision and GMBus Base Address

Address Offset: 00h
Default Value: {1010***, 0010,*** 0 GPIO[8] GPIO[7] 0, 0010}
Access: Read only

| Bit | Description |
|---|---|
| 15:12 | 82807AA VCH identification (Ah for VCH) |
| 11:8 | 82807AA ***VCH revision number***<br>**VCH A0 = 0h**<br>**VCH A1 = 1h**<br>**VCH A2 = 2h** |
| 7 | Reserved |
| 6:0 | VCH GMBus base address<br>Possible base address are 62h, 42h, 22h, or 02h depending on GPIO[8:7] strapping.<br>VR00[6] = the strapping value of GPIO[8]<br>VR00[5] = the strapping value of GPIO[7]<br>VR00[4:0] = 00010b |

***Note:*** **The VCH GMBus base address for straping starts at 02h, from bits 4:0. GPIO 7 and GPIO 8 determine the two MSB's:**

| Address | GPIO 08 | GPIO 07 |
|---|---|---|
| 02h | 0 | 0 |
| 22h | 0 | 1 |
| 42h | 1 | 0 |
| 62h | 1 | 1 |

## 2. Change to CMOS Panel Interface Drive Strength

*Section 6.1.2.2. (Page 38) should be replaced by:*

### VR11 – CMOS Output Control

Address offset: 11h
Default: 0000h
Access: Read/Write

| Bit | Description |
|---|---|
| 15 | Reserved |
| 14 | Shift clock mask.<br>0 = Allows shift clock output to toggle outside the display enable interval.<br>1 = Force shift clock output low outside the display enable interval. |
| 13 | Force LP during vertical blank.<br>0 = LP is active during vertical blank time.<br>1 = LP is inactive during vertical blank time. |
| 12 | Force DE during vertical blank.<br>0 = DE is inactive during vertical blank time.<br>1 = DE is active during vertical blank time. |
| 11:10 | Reserved |
| 9 | LCD panel interface group: P[35:0] signals (as a group)<br>0 = no inversion<br>1 = invert sense of signal |
| 8 | LCD panel interface group: SHFCLK signal<br>0 = no inversion<br>1 = invert sense of signal |
| 7 | LCD panel interface group: FLM signal<br>0 = no inversion<br>1 = invert sense of signal |
| 6 | LCD panel interface group: LP signal<br>0 = no inversion<br>1 = invert sense of signal |
| 5 | LCD panel interface group: DE signal<br>0 = no inversion<br>1 = invert sense of signal |
| 4:2 | Reserved |
| 1 | LCD timing controls and clock (FLM, LP, DE, and SHFCLK) output buffer strength.<br>0 = lower drive **(8 mA)**<br>1 = higher drive **(14 mA)** |
| 0 | LCD data (P[35:0]) output buffer strength.<br>0 = lower drive **(8 mA)**<br>1 = higher drive **(14 mA)** |

## 3. Change to Control Registers VR31 and VR32

Section 6.1.5.2. (Page 43) and Section 6.1.5.3. (Page 44) should be replaced by:

### VR31 – Tpon Panel Power On Sequencing Delay

Address offset: 31h
Default: 0200h
Access: Read/Write

| Bit | Description |
|---|---|
| 15:12 | Reserved |
| ***11:7*** | ***Power up delay Tpdatobkl: VR32[11:7] & VR31[11:7] is the 10-bit programmable value of panel power sequencing delay Tpdatobkl. This value can be programmed up to 1024ms in increments of ~1 millisecond (0.98304 ms actual). VR31[11:7] are the LSB. A value of 0 is undefined/implementation specific and should be avoided by programmers.*** |
| 6:0 | Power up delay: Tpon. Programmable value of panel power sequencing delay during power up. This value can be programmed up to ***128ms*** in increments of ~1 millisecond (0.98304 ms actual). A value of 0 is undefined/implementation specific and should be avoided by programmers. |

### VR32 – Tpoff Panel Power Off Sequencing Delay

Address offset: 32h
Default: 0200h
Access: Read/Write

| Bit | Description |
|---|---|
| 15:12 | Reserved |
| ***11:7*** | ***Power up delay Tpdatobkl: VR32[11:7] & VR31[11:7] is the 10-bit programmable value of panel power sequencing delay Tpdatobkl. This value can be programmed up to 1024ms in increments of ~1 millisecond (0.98304 ms actual). VR32[11:7] are the MSB. A value of 0 is undefined/implementation specific and should be avoided by programmers.*** |
| 6:0 | Power down delay: Tpoff. Programmable value of panel power sequencing delay during power down. This value can be programmed up to ***~128ms*** in increments of ~1 millisecond (0.98304 ms actual). A value of 0 is undefined/implementation specific and should be avoided by programmers. |

## 4. Change to Control Register VR34

*In Section 6.1.5.6 (Page 45) should be replaced by:*

### VR34 – Maximal FLM Pulse Interval

Address offset: 0034h
Default: 0001h
Access: Read/Write

| Bit | Description |
|---|---|
| 15:14 | Reserved |
| 13:0 | Maximal FLM pulse interval in display lines. If no FLM is generated from FPtg when the maximal FLM pulse interval is reached, VCH panel protection state machine generates FLM automatically. This register is normally programmed to a value which is less than but close to the maximal allowance of the installed panel. |

## 5. Change to Timing Control

Revise to Section 8.1.1

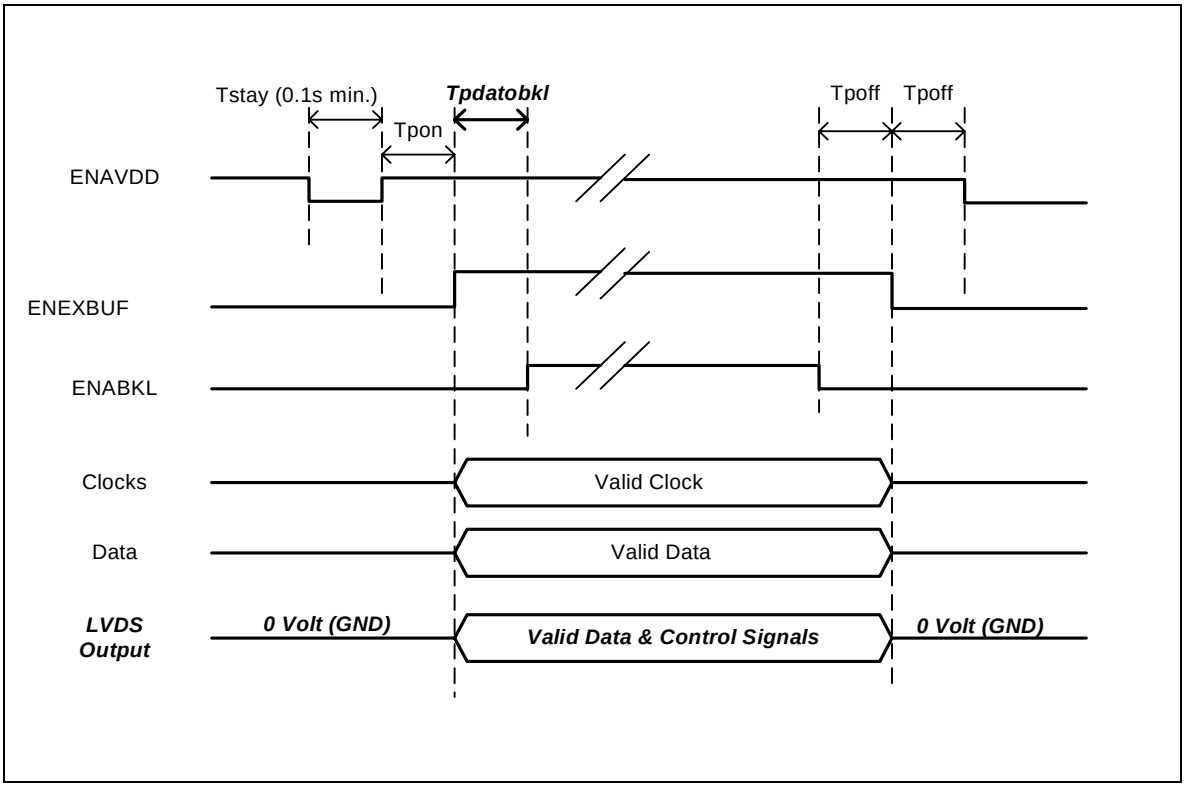
## 8.1. Timing Reference Point Generation

DVO timing tracks the X and Y coordinates of a DVO display frames, and generates horizontal and vertical Timing Reference Point (TRP) according to the DVO X and Y coordinates. VCH generates vertical display enable (V_DE) by monitoring DVOBLANK#. The horizontal and vertical TRP, as well as V_DE, are then synchronize to LCD clock domain for FP timing.

## 6. Change to Intel 82807AA VCH Panel Sequencing Diagram

*In Section 7.4.1.1 (Page 57) Figure 14 should be replaced with:*

**Figure 1. Panel Sequencing Diagram**



## 7. Calculation to Control Registers VR31 and VR32, Power Sequencing

In Figure 1, the Tpdatobkl , Tpon, and Tpoff delays are controlled by the values programmed in VR31 and VR32. These values must comply with the chosen installed panel specification. The actual Tpdatobkl , Tpon, Tpoff, and other delays are based on OSC clock input. These delay value can be programmed to increments of ~1 millisecond. A value of 0 is undefined/implementation specific and should be avoided by programmers. Refer to the latest datasheet and specification update for more information on registers VR31 and V32 of the VCH.

**Actual Delay Table**

| OSC Clock | CMOS | LVDS |
|---|---|---|
| 66MHz | 0.990 ms | 0.730 ms |
| 48MHz | 1.375 ms | 1.000 ms |

Here is an *example* how to of calculate and specify a panel's Tpdatobkl , Tpon, and Tpoff delay values.

| | LVDS | CMOS | VR31[6:0] | VR32[6:0] |
|---|---|---|---|---|
| Tpon | 92ms | 126ms | 1111111b | |
| Tpoff | 10ms | 15ms | | 0001110b |
| | | | VR31[11:7] | VR32[11:7] |
| Tpdatobkl | 184ms | 253ms | 00000b | 01000b |

If the selected LCD panel requires 92ms for Tpon, and 10ms for tpoff, follow the calculation below.

92ms / 0.73ms = 127d = 1111111b

10ms / 0.73ms = 14d = 0001110b

Therefore the VR31[15:0] should be 007Fh and the VR32[15:0] should be 040Eh.

# Specification Clarifications

## 1. LVDS LCD Interface Pixel Data Serial Mapping

Revise to table's titles only in section 9.2

**Table 19. LVDS Conventional Data Mapping for 1x18 Interface (for panels with single channel)**

| LVDS Pair | 1st Data | 2nd Data | 3rd Data | 4th Data | 5th Data | 6th Data | 7th Data |
|---|---|---|---|---|---|---|---|
| CLKA | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YA0 | Gn[0] | Rn[5] | Rn[4] | Rn[3] | Rn[2] | Rn[1] | Rn[0] |
| YA1 | Bn[1] | Bn[0] | Gn[5] | Gn[4] | Gn[3] | Gn[2] | Gn[1] |
| YA2 | DE | FLM | LP | Bn[5] | Bn[4] | Bn[3] | Bn[2] |
| YA3 | Disabled | | | | | | |
| CLKB | Disabled | | | | | | |
| YB0 | Disabled | | | | | | |
| YB1 | Disabled | | | | | | |
| YB2 | Disabled | | | | | | |
| YB3 | Disabled | | | | | | |

**Table 20. LVDS Conventional Data Mapping for 2x18 Interface (for panels with dual channels)**

| LVDS Pair | 1st Data | 2nd Data | 3rd Data | 4th Data | 5th Data | 6th Data | 7th Data |
|---|---|---|---|---|---|---|---|
| CLKA | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YA0 | Gn[0] | Rn[5] | Rn[4] | Rn[3] | Rn[2] | Rn[1] | Rn[0] |
| YA1 | Bn[1] | Bn[0] | Gn[5] | Gn[4] | Gn[3] | Gn[2] | Gn[1] |
| YA2 | DE | FLM | LP | Bn[5] | Bn[4] | Bn[3] | Bn[2] |
| YA3 | Disabled | | | | | | |
| CLKB | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YB0 | Gn+1[0] | Rn+1[5] | Rn+1[4] | Rn+1[3] | Rn+1[2] | Rn+1[1] | Rn+1[0] |
| YB1 | Bn+1[1] | Bn+1[0] | Gn+1[5] | Gn+1[4] | Gn+1[3] | Gn+1[2] | Gn+1[1] |
| YB2 | 0 | 0 | 0 | Bn+1[5] | Bn+1[4] | Bn+1[3] | Bn+1[2] |
| YB3 | Disabled | | | | | | |

**NOTES:**
1. n denotes to nth pixel data.
2. R, G, B denote to the red, green, blue color elements in a pixel.
3. Based on naming conventions, 18 bpp to 24 bpp are mapped as follows, and bit 0 in each color element is the LSB of the gray scale.

**Table21. LVDS Conventional Data Mapping for 1x24 Interface (for panels with single channel)**

| LVDS Pair | 1st Data | 2nd Data | 3rd Data | 4th Data | 5th Data | 6th Data | 7th Data |
|---|---|---|---|---|---|---|---|
| CLKA | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YA0 | Gn[2] | Rn[7] | Rn[6] | Rn[5] | Rn[4] | Rn[3] | Rn[2] |
| YA1 | Bn[3] | Bn[2] | Gn[7] | Gn[6] | Gn[5] | Gn[4] | Gn[3] |
| YA2 | DE | FLM | LP | Bn[7] | Bn[6] | Bn[5] | Bn[4] |
| YA3 | 0 | Bn[1] | Bn[0] | Gn[1] | Gn[0] | Rn[1] | Rn[0] |
| CLKB | Disabled | | | | | | |
| YB0 | Disabled | | | | | | |
| YB1 | Disabled | | | | | | |
| YB2 | Disabled | | | | | | |
| YB3 | Disabled | | | | | | |

**Table 22. LVDS Conventional Data Mapping for 2x24 Interface (for panels with dual channels)**

| LVDS Pair | 1st Data | 2nd Data | 3rd Data | 4th Data | 5th Data | 6th Data | 7th Data |
|---|---|---|---|---|---|---|---|
| CLKA | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YA0 | Gn[2] | Rn[7] | Rn[6] | Rn[5] | Rn[4] | Rn[3] | Rn[2] |
| YA1 | Bn[3] | Bn[2] | Gn[7] | Gn[6] | Gn[5] | Gn[4] | Gn[3] |
| YA2 | DE | FLM | LP | Bn[7] | Bn[6] | Bn[5] | Bn[4] |
| YA3 | 0 | Bn[1] | Bn[0] | Gn[1] | Gn[0] | Rn[1] | Rn[0] |
| CLKB | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| YB0 | Gn+1[2] | Rn+1[7] | Rn+1[6] | Rn+1[5] | Rn+1[4] | Rn+1[3] | Rn+1[2] |
| YB1 | Bn+1[3] | Bn+1[2] | Gn+1[7] | Gn+1[6] | Gn+1[5] | Gn+1[4] | Gn+1[3] |
| YB2 | 0 | 0 | 0 | Bn+1[7] | Bn+1[6] | Bn+1[5] | Bn+1[4] |
| YB3 | 0 | Bn+1[1] | Bn+1[0] | Gn+1[1] | Gn+1[0] | Rn+1[1] | Rn+1[0] |

## 2. Clarification to the VCH GMBUS Strapping

See Specification Change *1. Intel 82807AA VCH Revision VR00 Register Description* for more information.

## 3. Clarification of register VR01[2]

### VR01 - 82807AA VCH Functionality Enable

Address offset: 01h
Default: 0000h
Access: Read/write

| Bit | Description |
|---|---|
| 15:5 | Reserved |
| 4 | Reserved |
| 3 | Panel Fitting enabled. This bit enables or disables (bypassing) 82807AA VCH panel fitting function when LCD display is enabled.<br><br>0 = disabled<br>1 = enabled |
| 2 | LCD display enabled. This bit enables or disables 82807AA VCH LCD display function.<br><br>0 = disabled<br>1 = enabled<br><br>This bit can only be set to 1 if VR01[1] is set to 0, due to there is only one PLL for either LCD display or DVO bypassing.<br><br>When setting this bit to 1, software must assume a 25 millisecond delay from the time the command is executed in code to the rise of $ENAV_{DD}$.<br><br>ENABKL must be active before changing this bit from 1 to 0. |
| 1 | DVO bypassing enable. This bit enables or disables 82807AA VCH DVOr port.<br><br>0 = disabled<br>1 = enabled<br><br>When DVOr is enabled, it repeats the signaling of DVO. When it is disabled, all DVOr outputs are driven to low, and all DVOr inputs are ignored. This bit can only be set to 1 if VR01[2] is set to 0, due to there is only one PLL for either LCD display or DVO bypassing. |
| 0 | DVO enable. This bit controls all functions in DVO clock domain by gating the clock of 82807AA VCH DVO clock domain.<br><br>0 = disabled<br>1 = enabled |

## 4. Clarification of register VR30[15]

### VR30 - Panel Power Shut Down Status

Address offset: 30h
Default: 0000h
Access: Read only for [15], Read/write for the rest

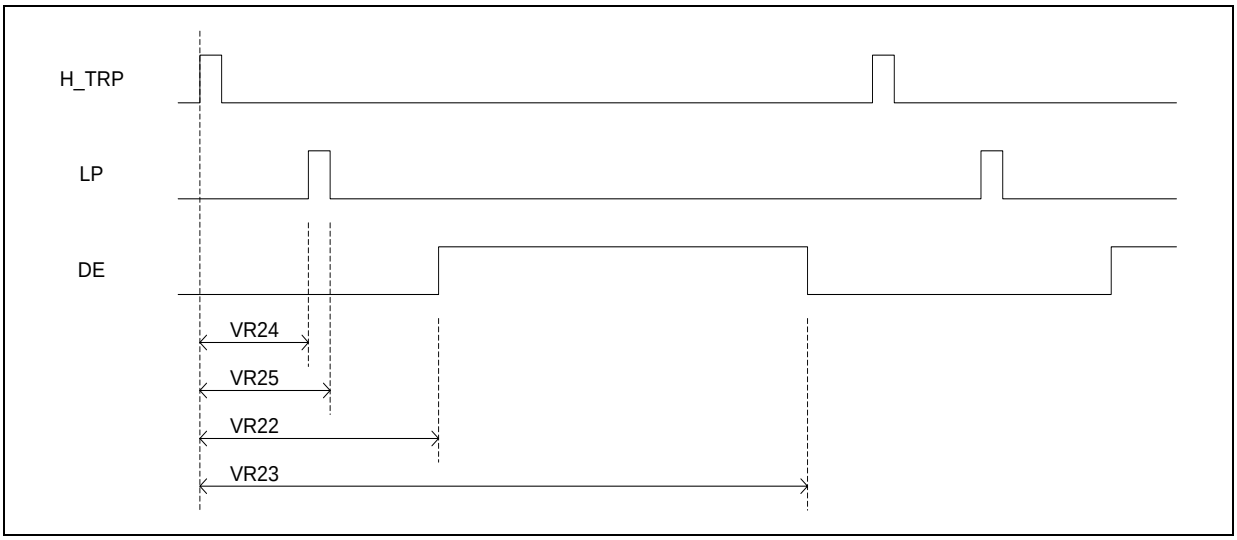
| Bit | Description |
|---|---|
| 15:15 | 0 = It is safe to program panel timing and PLL registers in 82807AA VCH.<br>1 = It is unsafe to program panel timing and PLL registers in 82807AA VCH.<br>Note: This bit is read only.<br>This bit is set when VR01[2] is set to "1". It is not an indication that the Tpon or Tpdatobkl timers have elapsed.<br>This bit is cleared (set to "0") when VR01[2] has been set to "0", and the Tpoff timers have elapsed (i.e. ENAVDD has been de-asserted). It is not an indication of the status of the Tstay timer.<br>Software is responsible to enable LCD display by writing a "1" to VR01[2] after all panel timing and PLL registers are programmed.<br>It is also SW responsibility to check this bit before panel timing and PLL registers programming. |
| 14:0 | Reserved. |

# Documentation Changes

## 1. Correct Flat Panel Timing Diagram

*In Section 8.1.1.1 (Page 52) Figure 10 should be replaced with:*

**Figure 2. LP and DE With respect to H_TRP**



## 2. Correction to Table 18, CMOS Flat Panel Out

Section 9.1, Table 18 should be replaced with:

**Table 18. CMOS Flat Panel Out**

| Pin Name | 1x24 | 2x18 | 1x18 |
|---|---|---|---|
| P0 | Bn[0] | Bn[0] | |
| P1 | Bn[1] | Bn[1] | |
| P2 | Bn[2] | Bn[2] | Bn[0] |
| P3 | Bn[3] | Bn[3] | Bn[1] |
| P4 | Bn[4] | Bn[4] | Bn[2] |
| P5 | Bn[5] | Bn[5] | Bn[3] |
| P6 | Bn[6] | Bn+1[0] | Bn[4] |
| P7 | Bn[7] | Bn+1[1] | Bn[5] |
| P8 | Gn[0] | Bn+1[2] | |
| P9 | Gn[1] | Bn+1[3] | |
| P10 | Gn[2] | Bn+1[4] | Gn[0] |
| P11 | Gn[3] | Bn+1[5] | Gn[1] |
| P12 | Gn[4] | Gn[0] | Gn[2] |
| P13 | Gn[5] | Gn[1] | Gn[3] |
| P14 | Gn[6] | Gn[2] | Gn[4] |
| P15 | Gn[7] | Gn[3] | Gn[5] |
| P16 | Rn[0] | Gn[4] | |
| P17 | Rn[1] | Gn[5] | |
| P18 | Rn[2] | Gn+1[0] | Rn[0] |
| P19 | Rn[3] | Gn+1[1] | Rn[1] |
| P20 | Rn[4] | Gn+1[2] | Rn[2] |
| P21 | Rn[5] | Gn+1[3] | Rn[3] |
| P22 | Rn[6] | Gn+1[4] | Rn[4] |
| P23 | Rn[7] | Gn+1[5] | Rn[5] |

| Pin Name | 1x24 | 2x18 | 1x18 |
|---|---|---|---|
| P24 | | Rn[0] | |
| P25 | | Rn[1] | |
| P26 | | Rn[2] | |
| P27 | | Rn[3] | |
| P28 | | Rn[4] | |
| P29 | | Rn[5] | |
| P30 | | Rn+1[0] | |
| P31 | | Rn+1[1] | |
| P32 | | Rn+1[2] | |
| P33 | | Rn+1[3] | |
| P34 | | Rn+1[4] | |
| P35 | | Rn+1[5] | |

**NOTES:**
1. n denotes to the nth pixel data
2. R, G, B, denote to the red, green, and blue color elements in a pixel and bit 0 is LSB.

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